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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/390,090	LEVESQUE ET AL.	
	Examiner	Art Unit	
	Michael W. Hoye	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-11,14-16,18-25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11,14-16,18-25 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 September 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicants' arguments filed on November 12, 2004 regarding claims 1, 20-23, 4, 8, 11 and 29 have been fully considered but they are not persuasive.

Regarding independent claim 1, the Applicants argue that, "O'Connor and Yonemitsu, alone or in combination, do not teach or suggest steps for (i) a first buffering of an input signal having a digital video format and (ii) compressing the input signal in parallel with the first buffering as presently claimed."

In response, the Examiner respectfully disagrees with the Applicants because while the O'Connor reference does not explicitly show a first buffering of an input signal having a digital video format and compressing the input signal in parallel with the first buffering. O'Connor does disclose in col. 2, lines 3-12, that if the incoming video stream is an analog stream, such as analog NTSC signals, VIDEO IN 102 performs an A to D function (analog to digital) that takes the analog signals and converts them into a digital video bit stream, which may involve buffering the video stream. In addition to, it would have been clearly obvious to one of ordinary skill in the art to have provided a frame buffer along the real-time video bypass path 142, which is in parallel with the compression stage 104 (Fig. 1), for the advantage of providing a smooth transition between the time-shifted video stream coming from the decompression stage 110 to the video out 120, and the real-time video stream sent along bypass path 142 to the video out 120. One of ordinary skill in the art would have been led to make such a modification since the video stream transmitted along the time-shifted video stream path (which begins at an output of

video in 102, then proceeds through the compression unit 104, continues though several other units as shown in Fig. 1 and eventually is output to video out 120) would encounter a minimal delay or lag upon arriving at video out 120, in relation to the real-time video stream transmitted along bypass 142, even if no time-shift was requested by a viewer, because of the additional processing required by the compression, decompression, and other buffer and storage units. Therefore, a buffer would need to be provided in the real-time video stream bypass path 142 in order to account for the lag or delays due to the additional processing along the time-shifted video stream path so that the real-time video path would be delayed enough to overcome or provide a smooth transition from the time-shifted path, such as when a viewer causes the playback of the time-shifted video stream to fall within a certain threshold, wherein the system 100 will cease providing the time-shifted video stream and switch to incoming or real-time video stream provided along bypass 142 (col. 4, lines 46-58).

As an additional note, the Yonemitsu reference was provided to show that it is well known in the art to provide a frame buffer prior to a compression stage.

Regarding claim 1, the Applicants also argue that, "the proposed combination of O'Connor and Yonemitsu appears to be silent regarding a video in block 102 of O'Connor providing video frames as buffered along a bypass 142.

In response, the Examiner respectfully disagrees with the Applicants for the same reasons as described in the paragraphs above.

Also regarding independent claim 1, the Applicants further argue that, "The assertion on page 7 of the Office Action that buffering and compressing inherently occur substantially simultaneously is respectfully traversed and should be withdrawn..."

In response, the Examiner respectfully disagrees with the Applicants because the arguments made are moot since the claim was amended and no longer includes the words "substantially simultaneously".

Regarding independent claim 20, the Applicants argue that:

> "the video in 102 block of O'Connor (asserted similar to the claimed real-time decoder) does not appear to have (i) a decompression capability or (ii) a frame pause capability. Therefore, O'Connor does not teach or suggest a real-time decoder configured to (i) generate a first output signal by decompressing a compressed digital video input signal and (ii) pause a frame of the first output signal during a transition from a first mode to a second mode as presently claimed."

In response, the Examiner respectfully disagrees with the Applicants because the claimed real-time decoder configured to (i) generate a first output signal by decompressing a compressed digital video input signal is met by the O'Connor reference which discloses that in one embodiment the input video stream received at Video In 102 is already compressed, such as a video stream that is a MPEG 2 video signal (col. 2, lines 16-20). Moreover, as shown in Fig. 1, when a video stream that is uncompressed is received and is processed through the time shifting circuitry including the compression stage 104, the video stream must be decompressed at the decompression 110 section before being sent to video out 120, in order to be able to view the video stream on the display. In addition to, *Newton's Telecom Dictionary* defines decompression as, "The process of expanding a compressed image or file so it can be viewed, printed, faxed or otherwise processed." Therefore, regarding the real-time path (bypass 142), it is well known that the video in 102 would have to send the real-time signal intended for bypass 142 through a decompressor in order to convert the compressed MPEG 2 stream for output to a television through video out 120 via bypass 142 for the disclosed embodiment of receiving a

compressed MPEG 2 stream. Although a decompressor is not explicitly shown in the figure for the real time path (bypass 142), it is well known that one would be used before the video signal is received by video out 120 as described above. The claimed (ii) pause a frame of said first output signal during a transition from a first mode to a second mode is specifically met by the VIDEO OUT providing a still image at the VIDEO OUT when the user signals a command from the remote control to suspend the display of the incoming video stream (see col. 4, line 65 – col. 5, line 19).

The Applicants also argue that, "Nothing in O'Connor indicates that the bypass 142 is available for all configurations, including the compressed video input/uncompressed video output configuration asserted in the Office Action."

In response, the Examiner respectfully disagrees with the Applicants because nothing in O'Connor indicates that the bypass is not available either. O'Connor already discloses the bypass as described above and the Examiner has clearly indicated why one of ordinary skill in the art would have a decoder in the bypass 142 for a compressed video input situation as previously described above. Since O'Connor has already disclosed bypass 142 for at least one embodiment, it would have been obvious to use the bypass in other embodiments for the reasons given above.

Furthermore, the Applicants argue that, "the Office Action provides no evidence of motivation to modify O'Connor..."

In response, the Examiner respectfully disagrees with the Applicants because the O'Connor reference must have a decompression capability in order to view a compressed video stream as previously described above. As previously stated, O'Connor discloses that the input

video stream received at Video In 102 may already be compressed, such as a video stream that is a MPEG 2 video signal (col. 2, lines 16-20). Moreover, as shown in Fig. 1, when a video stream that is uncompressed is received and is processed through the time shifting circuitry including the compression stage 104, the video stream must be decompressed at the decompression 110 section before being sent to video out 120. Therefore, regarding the real-time path (bypass 142), it is well known that the video in 102 would have to send the real-time signal intended for bypass 142 through a decompressor in order to convert the compressed MPEG 2 stream for output to a television through video out 120 via bypass 142 for the disclosed embodiment of receiving a compressed MPEG 2 stream. Although a decompressor is not explicitly shown in the figure for the real time path (bypass 142), it is well known that one would be used before the video signal is received by video out 120 (also see the *Newton's Telecom Dictionary* definition of **decompression** as stated above). Finally, it would have been obvious to combine the video in block 102 of O'Connor with the video out block of O'Connor in order to reduce the number of parts in the system and further simplify the amount of components needed to build the system.

As to independent claim 21, the Applicants argue that, "...no evidence of motivation is provided in the Office Action to add a frame buffer to Thomason."

In response, the Examiner has provided evidence of the motivation that a frame buffer may be directly connected to said input...as disclosed in the previously cited reference of Yonemitsu et al (USPN 5,510,840), where the reference clearly teaches that a frame buffer memory 18, as shown in Fig. 23, may be used at the input in order to provide a smooth transition when switching between signals for a change of mode, as well as providing buffering to account for variations in the timing of the video stream before reaching the compression stage. The

buffering (buffer memory 18) occurs just prior to the compression stage (elements receiving the contents of buffer memory 18), in order to properly perform the encoding or compression of the input video signal comprised of picture data of a picture (field or frame), which includes motion prediction and other processes (see col. 13, lines 18-47). Other buffers are shown in elements 7, 8 and 26. Therefore, it would have been obvious to one of ordinary skill in the art of video processing and compression to have combined the Thomason reference, which teaches compression prior to storage, with the teachings of Yonemitsu et al, which teaches buffering the input signal prior to the compression stage for the advantages of storing picture or frame data in a buffer memory in order to perform the necessary encoding or compression operations, such as detecting a motion vector for motion prediction, in addition to actually compressing the stream and providing for smooth transmission of the stream after compression. One of ordinary skill in the art would have been led to make such a modification since buffering an input signal prior to the compression stage is well known in the art of video compression as described above.

The Applicants further argue that, "the proposed modification of Thomason does not appear to teach or suggest an encoder configured to generate a first intermediate signal by compressing the video signal as presently claimed."

In response, the Examiner respectfully disagrees with the Applicants for the reasons described above as related to the combination of the Thomason and Yonemitsu references.

The Applicants also argue that, "page 16 of the Office Action asserts that one of ordinary skill in the art would consider a buffer 4 of Thomason to be similar to the claimed controller."

In response, the Examiner respectfully disagrees with the Applicants because page 16 of the previous Office Action clearly states that:

> "The claimed controller separate from said encoder and configured to (i) receive said first intermediate signal and (ii) present a second intermediate signal is met by **elements 4, 31-33, 14 and 21-25** as shown in Fig. 1, where the first intermediate signal is received at buffers 4 and the second intermediate signal is presented at the output of buffers 14 and is sent to data decompressor or decoder 13."

The claimed controller is represented by **elements 4, 31-33, 14 and 21-25**, not just element 4 as stated by the Applicants. Therefore, the rejection has been maintained as previously presented.

The Applicants also argue that:

> "FIG. 1 of Thomason shows that a buffer memory 35 (asserted similar to the claimed frame storage system) is indirectly connected to a buffer 4 (asserted similar to the claimed controller) through a DMA controller 31. Therefore, Thomason does not appear to teach or suggest a frame storage system directly connected to the controller and configured to (i) store a first intermediate signal and (ii) generate a second intermediate signal as presently claimed."

In response, the Examiner respectfully disagrees with the Applicants because page 16 of the previous Office Action clearly states that:

> "The claimed frame storage system directly connected to said controller and configured to (i) store said first intermediate signal and (ii) generate said second intermediate signal is met by buffer memory 35 and main memory 36 (Fig. 1, col. 3, line 53 – col. 4, line 40), which receives the first intermediate signal from 31 and the second intermediate is generated at the output data section of 35."

The claimed controller is represented by **elements 4, 31-33, 14 and 21-25**, as described above, not just element 4 as previously stated by the Applicants. Therefore, the rejection has been maintained as previously presented.

Finally, regarding claim 21, the Applicants also argue that:

> "Assuming, *arguendo*, that a frame buffer was added to the design of Thomason (for which Applicants' representative does not necessarily

> agree), nothing in the proposed modified design appears to teach or suggest a first output signal from the frame buffer being presented while in a first mode."

In response, the Examiner respectfully disagrees because of the Yonemitsu et al reference's teaching regarding a frame buffer as previously described above in combination with Thomason, as well as, the teachings of Thomason as previously described by the Examiner where the first output signal is met by the live selection(s) path as shown in Fig. 1, the claimed time-shifted video decoder separate from said controller and configured to generate a second output signal by decompressing said second intermediate signal is met by data decompressor 13 (Fig. 1), which generates the second output signal that is sent through the acceleration control 41 and PIP/postprocessor 42 to a TV (col. 4, lines 15-40), and the claimed wherein said controller is further configured to generate a command configured to control presenting (i) the first output signal when in the first mode and (ii) a second output signal when in a second mode is met by the live selection(s) path as shown in Fig. 1 for the first output signal, as well as the microprocessor 24 and the user command input ports 25 as part of the overall controller as described above, in conjunction with the acceleration control 41 and PIP/postprocessor 42 (see Fig. 1 and col. 3, line 58 – col. 4, line 40).

As to independent claim 22, the Applicants argue that:

> "the video in 102 block of O'Connor (asserted similar to the claimed real-time decoder) does not appear to have (i) a decompression capability or (ii) a frame pause capability. Therefore, O'Connor does not teach or suggest a real-time decoder configured to (i) generate a first output signal by decompressing a compressed digital video input signal and (ii) pause a frame of the first output signal during a transition from a first mode to a second mode as presently claimed."

In response, the Examiner respectfully disagrees with the Applicants because the claimed real-time decoder configured to (i) generate a first output signal by decompressing a compressed digital video input signal is met by the O'Connor reference which discloses that in one embodiment the input video stream received at Video In 102 is already compressed, such as a video stream that is a MPEG 2 video signal (col. 2, lines 16-20). Moreover, as shown in Fig. 1, when a video stream that is uncompressed is received and is processed through the time shifting circuitry including the compression stage 104, the video stream must be decompressed at the decompression 110 section before being sent to video out 120, in order to be able to view the video stream on the display. In addition to, *Newton's Telecom Dictionary* defines decompression as, "The process of expanding a compressed image or file so it can be viewed, printed, faxed or otherwise processed." Therefore, regarding the real-time path (bypass 142), it is well known that the video in 102 would have to send the real-time signal intended for bypass 142 through a decompressor in order to convert the compressed MPEG 2 stream for output to a television through video out 120 via bypass 142 for the disclosed embodiment of receiving a compressed MPEG 2 stream. Although a decompressor is not explicitly shown in the figure for the real time path (bypass 142), it is well known that one would be used before the video signal is received by video out 120 as described above. The claimed (ii) pause a frame of said first output signal during a transition from a first mode to a second mode is specifically met by the VIDEO OUT providing a still image at the VIDEO OUT when the user signals a command from the remote control to suspend the display of the incoming video stream (see col. 4, line 65 – col. 5, line 19).

The Applicants also argue that, "Nothing in O'Connor indicates that the bypass 142 is available for all configurations, including the compressed video input/uncompressed video output configuration asserted in the Office Action."

In response, the Examiner respectfully disagrees with the Applicants because nothing in O'Connor indicates that the bypass is not available either. O'Connor already discloses the bypass as described above and the Examiner has clearly indicated why one of ordinary skill in the art would have a decoder in the bypass 142 for a compressed video input situation as previously described above. Since O'Connor has already disclosed bypass 142 for at least one embodiment, it would have been obvious to use the bypass in other embodiments for the reasons given above.

Furthermore, the Applicants argue that, "the Office Action provides no evidence of motivation to modify O'Connor..."

In response, the Examiner respectfully disagrees with the Applicants because the O'Connor reference must have a decompression capability in order to view a compressed video stream as previously described above. As previously stated, O'Connor discloses that the input video stream received at Video In 102 may already be compressed, such as a video stream that is a MPEG 2 video signal (col. 2, lines 16-20). Moreover, as shown in Fig. 1, when a video stream that is uncompressed is received and is processed through the time shifting circuitry including the compression stage 104, the video stream must be decompressed at the decompression 110 section before being sent to video out 120. Therefore, regarding the real-time path (bypass 142), it is well known that the video in 102 would have to send the real-time signal intended for bypass 142 through a decompressor in order to convert the compressed MPEG 2 stream for output to a

television through video out 120 via bypass 142 for the disclosed embodiment of receiving a compressed MPEG 2 stream. Although a decompressor is not explicitly shown in the figure for the real time path (bypass 142), it is well known that one would be used before the video signal is received by video out 120 (also see the *Newton's Telecom Dictionary* definition of **decompression** as stated above). Finally, it would have been obvious to combine the video in block 102 of O'Connor with the video out block of O'Connor in order to reduce the number of parts in the system and further simplify the amount of components needed to build the system.

The Applicants also argue that:

> "Assuming, *arguendo*, that a compression block 104 and a decompression block 110 of O'Connor could be combined to form a frame storage system (for which Applicants' representative does not necessarily agree), the resulting combination does not appear to exchange a video input signal (in a compressed format) with a processor 130 of O'Connor (asserted similar to the claimed controller). In particular, FIG. 1 of O'Connor shows no exchange of video between the compression block 104 and/or decompression block of 110 of O'Connor with the processor 130. Furthermore, the video signal presented by the decompression block 110 of O'Connor is not in a compressed format."

In response, the Examiner respectfully disagrees with the Applicants because O'Connor clearly discloses in col. 2, lines 48-50 and in Fig. 1 that the functions of compression block 104 and decompression block 110 may be performed by the processor 130. Therefore, the compression block 104 and the decompression block 110 may exchange a compressed video input signal with the processor 130, and as stated in col. 2, lines 16-20 of O'Connor, if the video is already compressed no further compression is needed at compression block 104.

As to independent claim 23, the Applicants argue that, "Thomason appears to be silent regarding a frame buffer configured to buffer both an input signal and a third signal as presently claimed."

In response, the Examiner previously stated that it is well known in the art to use a frame buffer in order to provide a smooth transition when switching between output signals...(see pg. 16 of previous Office Action) and has provided evidence of the motivation that a frame buffer may be directly connected to said input...as disclosed in the previously cited reference of Yonemitsu et al (USPN 5,510,840), where the reference clearly teaches that a frame buffer memory 18, as shown in Fig. 23, may be used at the input in order to provide a smooth transition when switching between signals for a change of mode, as well as providing buffering to account for variations in the timing of the video stream before reaching the compression stage. The buffering (buffer memory 18) occurs just prior to the compression stage (elements receiving the contents of buffer memory 18), in order to properly perform the encoding or compression of the input video signal comprised of picture data of a picture (field or frame), which includes motion prediction and other processes (see col. 13, lines 18-47). Other buffers are also shown in elements 7, 8 and 26. Therefore, it would have been obvious to one of ordinary skill in the art of video processing and compression to have combined the Thomason reference, which teaches compression prior to storage, with the teachings of Yonemitsu et al, which teaches buffering the input signal prior to the compression stage for the advantages of storing picture or frame data in a buffer memory in order to perform the necessary encoding or compression operations, such as detecting a motion vector for motion prediction, in addition to actually compressing the stream and providing for smooth transmission of the stream after compression. One of ordinary skill in the art would have been led to make such a modification since buffering an input signal prior to the compression stage is well known in the art of video compression as described above.

The Applicants' additional arguments related to claim 23, as well as dependent claim 29, are moot due to the combination of the Thomason et al and Yonemitsu et al references.

As to dependent claim 4, the Applicants argue that, "Claim 4 provides a transition from a real-time mode to a time-shifted mode [that] is triggered by a single command of a viewer... [In contrast,] O'Connor appears to contemplate two user commands to transition between modes."

In response the Examiner respectfully disagrees with the Applicants because O'Connor clearly discloses the claimed **transition** mode is triggered by a single command of the viewer by the user selecting a function via the remote control, which triggers the **transition** from real-time to time-shifted (see col. 4, line 65 – col. 5, line 19).

As to dependent claim 8, the Applicants argue that, "Nothing in O'Connor indicates that the bypass 142 is available for all configurations, including the compressed video input/uncompressed video output configuration asserted in the Office Action."

In response, the Examiner respectfully disagrees with the Applicants because nothing in O'Connor indicates that the bypass is not available either. O'Connor already discloses the bypass as described above and the Examiner has clearly indicated why one of ordinary skill in the art would have a decoder in the bypass 142 for a compressed video input situation as previously described above. Since O'Connor has already disclosed bypass 142 for at least one embodiment, it would have been obvious to use the bypass in other embodiments for the reasons given above. It is well known that a decompressor would be used when the video in 102 receives an already compressed video stream such as a MPEG 2 video signal (col. 2, lines 16-20). If the user were operating in the live or real-time mode as discussed above the MPEG 2

signal would have to be decompressed before being sent to a television display (see *Newton's Telecom Dictionary* definition of decompression as previously stated).

As to dependent claim 11, the Applicants argue that, "O'Connor, Yonemitsu and Russo appear to be silent regarding a transition from one frame from the real-time frames to a subsequent frame from the time shifted frames."

In response the Examiner respectfully disagrees with the Applicants because the Russo reference was combined with O'Connor to provide explicit teaching as to a transition from one frame from the real-time frames to a subsequent frame from the time shifted frames. Russo et al discloses a method in which a memory is used for storing information relating to various points or frames in a program, so that at a specific point in a program when a "PAUSE command" (col. 3, lines 7-16 and col. 4, lines 15-27) is received, the system is automatically capable of commencing playback from that point or frame when a RESUME command is received beginning with the next frame. In another embodiment, when a "MARK command" (col. 3, lines 46-49) is issued and used along with "Marker memory" (col. 8, line 20), where information regarding program markers is stored to specify a point or frame from which playback can be resumed beginning with the next frame.

In addition, the Applicants argue that, "no evidence of motivation to combine the references is provided in the Office Action..."

In response to Applicants' argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the

knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner respectfully disagrees because the O'Connor reference discloses a method of time shifting a video stream and was used as the base reference, the Yonemitsu et al reference was provided for the teachings of memory buffers used in a compression stage, and the Russo et al reference also provides additional teachings for video time-shifting apparatus and methods regarding the transition between frames of video. One of ordinary skill in the art would have looked to the teachings of any one of these references since they are all in the art of video signal processing and more specifically, O'Connor and Russo are related to video time-shifting methods.

2. Regarding the Applicants' arguments that, "No arguments were developed for independent claim 23 and dependent claim 29."

The Examiner respectfully disagrees with the Applicants' assertion that the Examiner's action was incomplete. No arguments were developed for independent claim 23 and dependent claim 29 in the previous Office Action because of the new grounds of rejection presented by the Examiner.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Fig. 6 does not have a line from Host controller 20 to Switch 23, Figures 3 and 4 seem to indicate this feature. Therefore, the claimed wherein

said controller is further configured to generate a command configured to control presenting (i) said first output signal when in said first mode and (ii) said second output signal when in said second mode as claimed in claim 21, must be shown or the features canceled from the claim. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 7-10 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor (USPN 6,480,667), in view of Yonemitsu et al (USPN 5,510,840), both cited by the Examiner.

As to claim 1, note the O'Connor reference which discloses a time-shifted video method. The claimed first buffering of an input signal having a digital video format is met by the O'Connor reference which discloses in one embodiment that the Video In 102 is a video capture card (col. 2, lines 12-15), wherein it is well known that capture cards capture or buffer an input video signal for further processing before the video stream is sent to compression 104 or bypass 142, the video stream may be in digital form as met by col. 2, lines 11-12. The claimed compressing is met by compression 104 (Fig. 1, col. 2, lines 16-17 and col. 3, lines 37-38). While the O'Connor reference does not explicitly show a first buffering of an input signal having a digital video format and compressing the input signal in parallel with the first buffering. O'Connor does disclose in col. 2, lines 3-12, that if the incoming video stream is an analog stream, such as analog NTSC signals, VIDEO IN 102 performs an A to D function (analog to digital) that takes the analog signals and converts them into a digital video bit stream, which may involve buffering the video stream. In addition to, it would have been clearly obvious to one of ordinary skill in the art to have provided a frame buffer along the real-time video bypass path 142, which is in parallel with the compression stage 104 (Fig. 1), for the advantage of providing a smooth transition between the time-shifted video stream coming from the decompression stage 110 to the video out 120, and the real-time video stream sent along bypass path 142 to the video out 120. One of ordinary skill in the art would have been led to make such a modification since

the video stream transmitted along the time-shifted video stream path (which begins at an output of video in 102, then proceeds through the compression unit 104, continues though several other units as shown in Fig. 1 and eventually is output to video out 120) would encounter a minimal delay or lag upon arriving at video out 120, in relation to the real-time video stream transmitted along bypass 142, even if no time-shift was requested by a viewer, because of the additional processing required by the compression, decompression, and other buffer and storage units. Therefore, a buffer would need to be provided in the real-time video stream bypass path 142 in order to account for the lag or delays due to the additional processing along the time-shifted video stream path so that the real-time video path would be delayed enough to overcome or provide a smooth transition from the time-shifted path, such as when a viewer causes the playback of the time-shifted video stream to fall within a certain threshold, wherein the system 100 will cease providing the time-shifted video stream and switch to incoming or real-time video stream provided along bypass 142 (col. 4, lines 46-58). The Yonemitsu reference has been provided to show that it is well known in the art to provide a frame buffer prior to a compression stage, as well as during and after compression. The O'Connor reference does not explicitly show that the input signal is buffered then compressed. Yonemitsu et al specifically discloses this teaching as shown in Fig. 23, where buffering (buffer memory 18) occurs just prior to the compression stage (elements receiving the contents of buffer memory 18), as shown in Fig. 23, in order to properly perform the encoding or compression of the input video signal comprised of picture data of a picture (field or frame), which includes motion prediction and other processes (see col. 13, lines 18-47). Other buffers are shown in elements 7, 8 and 26. The claimed compressing including a second buffering of said input signal is met by Yonemitsu which also

discloses a second buffering as shown by transmission buffer memory 26. Therefore, it would have been obvious to one of ordinary skill in the art of video processing and compression to have combined the O'Connor reference, which teaches compression prior to storage, with the teachings of Yonemitsu et al, which teaches buffering the input signal prior to the compression stage, during compression, as well as after compression, for the advantages of storing picture or frame data in a buffer memory in order to perform the necessary encoding or compression operations, such as detecting a motion vector for motion prediction, in addition to actually compressing the stream and providing for smooth transmission of the stream after compression. One of ordinary skill in the art would have been led to make such a modification since buffering an input signal prior to the compression stage, as well as during and after, is well known in the art of video compression as described above. The claimed real-time mode, delivering a plurality of real-time video frames along a first processing path to an output for display in response to said input signal as first buffered is met in the O'Connor reference by the processing path from Video In 102, along Bypass 142, to Video Out 120 in Fig. 1 (col. 4, lines 54-57), where the "live" broadcast or incoming video stream is delivered to the video output 120. The claimed time-shifted mode, delivering a plurality of time-shifted video frames along a second processing path to said output for display...is met by the O'Connor reference, where the video input signal 102 (Fig. 1) is sent along the compression 104, buffer 106/storage 108, 122 units, decompression 110 and on to the video out 120 (see col. 2, line 54 – col. 3, line 2, as well as Fig. 2). The claimed said time-shifted video frames being delayed relative to said real-time video frames is met by retrieving a portion of the video stream from the storage unit while the recording of the incoming video stream continues, whereby the retrieved portion of the video stream is time-shifted from

the incoming video stream by a time delay (col. 2, lines 62-64 and col. 5, lines 2-19). The claimed pausing at a particular one of said real-time frames during a transition from said real-time mode to said time-shifted mode is met by the VIDEO OUT providing a still image at the VIDEO OUT when the user signals a command from the remote control to suspend the display of the incoming video stream (see col. 4, line 65 – col. 5, line 19).

As to claim 2, the claimed said transition is between said particular real-time frame and a time-shifted version of said particular real-time frame is met by the O'Connor reference, which discloses a user signaling the record and playback system 100 to suspend the display of the incoming or real-time video stream, wherein the VIDEO OUT provides a still image of the image present at the VIDEO OUT when the user signals a command from the remote control to suspend the display of the incoming video stream (see col. 4, line 65 – col. 5, line 19).

As to claim 3, O'Connor discloses various user commands or trick functions including "suspend" or pause, "un-suspend" or resume, "fast forward" and "rewind" which may be used during the time-shifted mode or delayed mode (see col. 4, line 65 – col. 5, line 53).

As to claim 4, O'Connor discloses that the claimed **transition** mode is triggered by a single command of the viewer by the user selecting a function via the remote control, which triggers the **transition** from real-time to time-shifted (see col. 4, line 65 – col. 5, line 19).

As to claims 5 and 7, O'Connor discloses that the real-time video frames (or video stream – received at VIDEO IN 102) may be derived from analog NTSC (uncompressed) video signals, digital, or digital compressed signals such as MPEG (col. 2, lines 5-20).

As to claim 8, the O'Connor reference discloses that the real-time video steam is decoded in the VIDEO IN 102 (Fig. 1, col. 2, lines 6-19). O'Connor discloses that the bypass 142 path is

for the real time or live video stream when the user is not buffering or recording the video stream for time-shifted operations (col. 4, lines 37-64). Although O'Connor does not explicitly show a decompressor along the bypass path 142, it is well known that a decompressor would be used when the video in 102 receives an already compressed video stream such as a MPEG 2 video signal (col. 2, lines 16-20). If the user were operating in the live or real-time mode as discussed above, the MPEG 2 signal would have to be decompressed before being sent to a television display.

As to claim 9, the O'Connor reference discloses that a processor 130 controls the operations of the video record and playback system 100 (i.e. the real-time mode, the time-shifted mode, and the transition), and the compression and decompression functions of units 104 and 110 may be performed by the processor 130 as well (col. 2, lines 45-52).

As to claim 10, O'Connor discloses that the input signal comprises MPEG video as described above in claim 7.

As to claim 24, O'Connor discloses that the transition is seamless to a viewer by pausing a frame of the video stream when the user signals a suspend or pause command to the video record and playback system 100 via a remote control, and when the user signals the video record and playback system 100 to un-suspend the video stream, it will play back at the point at which the video stream was suspended, where the video stream is time shifted by the amount of time that he suspended the incoming video stream, or the user may perform addition functions, such as fast forward or rewind through the time-shifted video stream (col. 5, lines 2-19). The pausing of the video stream provides a smooth or seamless transition from the real-time video stream to

the time-shifted video stream, as opposed to displaying a snowy screen, black or blue frames, or even intermittent video frames during the transition.

As to claim 25, the claimed transition is triggered by an event generated by software is met by the O'Connor reference where the user signals to the video record and playback system 100 to suspend the display of the incoming video stream and the firmware 140 (software within processor 130) controls the operations of the video record and playback system 100 to the suspending or pausing of a video frame and a transition to the time-shifted mode when a un-suspend or resume command is received (col. 2, lines 45-52 and col. 5, lines 2-18).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor, in view of Yonemitsu et al, in further view of Russo et al (USPN 5,701,383), all cited by the Examiner.

As to claim 11, the O'Connor reference discloses suspending or pausing a real-time video frame during a transition to a time-shifted mode as described above in claim 1. However, O'Connor does not give explicit detail as to information being stored identifying said particular real time video frame. Russo et al discloses a method in which a memory is used for storing information relating to various points or frames in a program, so that at a specific point in a program when a "PAUSE command" (col. 3, lines 7-16 and col. 4, lines 15-27) is received, the system is automatically capable of commencing playback from that point or frame when a RESUME command is received beginning with the next frame or, in another embodiment, when a "MARK command" (col. 3, lines 46-49) is issued and used along with "Marker memory" (col. 8, line 20), where information regarding program markers is stored to specify a point or frame

from which playback can be resumed beginning with the next frame. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to further include the teachings of Russo et al with O'Connor and Yonemitsu et al for the advantage of properly indexing and sequencing video frames in memory or storage for time-shifted mode queuing and to further provide smooth transitions when playback commences.

7. Claims 14, 20, 22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor.

As to claim 20, note the O'Connor reference which discloses an apparatus for time-shifting a real-time video stream. The claimed real-time decoder configured to (i) generate a first output signal by decompressing a compressed digital video input signal is met by the O'Connor reference which discloses that in one embodiment the input video stream received at Video In 102 is already compressed, such as a video stream that is a MPEG 2 video signal (col. 2, lines 16-20). Moreover, as shown in Fig. 1, when a video stream that is uncompressed is received and is processed through the time shifting circuitry including the compression stage 104, the video stream must be decompressed at the decompression 110 section before being sent to video out 120, in order to be able to view the video stream on the display. In addition to, *Newton's Telecom Dictionary* defines decompression as, "The process of expanding a compressed image or file so it can be viewed, printed, faxed or otherwise processed." Therefore, regarding the real-time path (bypass 142), it is well known that the video in 102 would have to send the real-time signal intended for bypass 142 through a decompressor in order to convert the compressed MPEG 2 stream for output to a television through video out 120 via bypass 142 for the disclosed

embodiment of receiving a compressed MPEG 2 stream. Although a decompressor is not explicitly shown in the figure for the real time path (bypass 142), it is well known that one would be used before the video signal is received by video out 120 as described above. The claimed (ii) pause a frame of said first output signal during a transition from a first mode to a second mode is specifically met by the VIDEO OUT providing a still image at the VIDEO OUT when the user signals a command from the remote control to suspend the display of the incoming video stream (see col. 4, line 65 – col. 5, line 19). It would have been obvious to combine the video in block 102 of O'Connor with the video out block of O'Connor in order to reduce the number of parts in the system and further simplify the amount of components needed to build the system. The claimed frame storage system configured to store said compressed digital video input signal separately from said real-time decoder is met by the compressed digital video signal being sent from VIDEO IN 102 (Fig. 1) through the compression 104 to buffer 106 and/or storage 108 and 122 units (see col. 2, line 54 – col. 3, line 2, as well as Figs. 1 and 2). The claimed time-shifted decoder is met by the decompression unit 110 (Fig. 1), which is coupled to said frame storage system 106, 108 and 122, and the decompression unit 110 generates a second output signal to video out 120 in response to said compressed digital video signal stored in said frame storage system. The claimed controller configured to generate a command configured to control presenting (i) said first output signal when in said first mode and (ii) said second output signal when in said second mode is met by processor 130 (Fig. 1, col. 2, lines 45-53 and col. 4, line 65 – col. 5, line 19).

As to claim 22, note the O'Connor reference which discloses an apparatus for time-shifting a real-time video stream. The claimed controller configured to receive a first command

and a video input signal in a compressed format is met by processor 130 (Fig. 1 and col. 2, lines 45-52), which may receive commands from a user via a remote control (col. 5, lines 2-5), and the processor 130 may also receive a video input signal in a compressed format (Fig. 1 and col. 2, lines 45-52). The claimed real-time decoder configured to (i) generate a first output signal in response to a decompressing a video input signal is met by the O'Connor reference which discloses that in one embodiment the input video stream received at Video In 102 is already compressed, such as a video stream that is a MPEG 2 video signal (col. 2, lines 16-20). Moreover, as shown in Fig. 1, when a video stream that is uncompressed is received and is processed through the time shifting circuitry including the compression stage 104, the video stream must be decompressed at the decompression 110 section before being sent to video out 120, in order to be able to view the video stream on the display. In addition to, *Newton's Telecom Dictionary* defines decompression as, "The process of expanding a compressed image or file so it can be viewed, printed, faxed or otherwise processed." Therefore, regarding the real-time path (bypass 142), it is well known that the video in 102 would have to send the real-time signal intended for bypass 142 through a decompressor in order to convert the compressed MPEG 2 stream for output to a television through video out 120 via bypass 142 for the disclosed embodiment of receiving a compressed MPEG 2 stream. Although a decompressor is not explicitly shown in the figure for the real time path (bypass 142), it is well known that one would be used before the video signal is received by video out 120 as described above. The claimed (ii) pause a frame of said first output signal during a transition from a first mode to a second mode is specifically met by the VIDEO OUT providing a still image at the VIDEO OUT when the user signals a command from the remote control to suspend the display of the incoming video stream

(see col. 4, line 65 – col. 5, line 19). The claimed frame storage system coupled to the controller to exchange said video input signal is met by the compression 104 and decompression 110 units as combined with the processor 130, which is coupled to the frame storage system 106 and 108 (see Fig. 1 and col. 2, lines 45-52). The claimed time shifted decoder is met by decompression 110, which is coupled to said controller (processor 130) as described above, and configured to generate a second output signal in response to the video input signal received from the controller and said first command is met by the decompression unit 110 generating a second output signal to video out 120 in response to said compressed digital video signal stored in said frame storage system and the first command received from the user as previously described above. In addition to, O'Connor clearly discloses in col. 2, lines 48-50 and in Fig. 1 that the functions of compression block 104 and decompression block 110 may be performed by the processor 130. Therefore, the compression block 104 and the decompression block 110 may exchange a compressed video input signal with the processor 130, and as stated in col. 2, lines 16-20 of O'Connor, if the video is already compressed no further compression is needed at compression block 104. The claimed controller is configured to generate a command configured to control presenting (i) said first output signal when in said first mode and (ii) said second output signal when in said second mode is met by processor 130 (Fig. 1, col. 2, lines 45-53 and col. 4, line 65 – col. 5, line 19).

As to claim 14, O'Connor does not disclose a real-time decoder and a time-shifted decoder that are provided in a single codec. However, the examiner takes Official Notice that it is notoriously well known in the art of interactive video distribution systems to integrate multiple components into a single component for the advantage of reducing manufacturing and

component costs, as well as simplifying the hardware design. Therefore, it is submitted that it would have been clearly obvious to one of ordinary skill in the art at the time of the invention to have provided the real-time decoder and time-shifted decoder in a single codec for the advantages given above.

As to claim 27, O'Connor does not explicitly disclose a demultiplexer configured to demultiplex said video input signal to said real-time decoder and said controller. However, the examiner takes Official Notice that it is notoriously well known in the art of interactive video distribution systems to incorporate the use of a demultiplexer to demultiplex video input signals for the advantage of allowing the apparatus to receive digital video signals which are normally transmitted in a multiplexed format, which allows for additional data capacity in the same amount of bandwidth. Therefore, it is submitted that it would have been clearly obvious to one of ordinary skill in the art at the time of the invention to have used a demultiplexer to demultiplex the input video signal in the apparatus for the advantages given above.

8. Claims 21, 15-16, 18-19, 23 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomason et al (USPN 6,018,612), in view of Yonemitsu et al (USPN 5,510,840), both previously cited by the Examiner.

As to claim 21, note the Thomason et al reference which discloses an apparatus (Fig. 1) for time-shifting a real-time video stream. The claimed input for receiving a video signal in an uncompressed format is met by the signals in arrow and channel selector 1 (see Fig. 1 and col. 3, lines 39-43). Although, the Thomason reference does not explicitly disclose a frame buffer directly connected to said input...it is well known in the art to use a frame buffer in order to

provide a smooth transition when switching between output signals for a change of mode, such as pausing a video output signal at a frame during transitions between modes. Moreover, Yonemitsu et al (USPN 5,510,840), clearly teaches that a frame buffer memory 18, as shown in Fig. 23, may be used at the input in order to provide a smooth transition when switching between signals for a change of mode, as well as providing buffering to account for variations in the timing of the video stream before reaching the compression stage. The buffering (buffer memory 18) occurs just prior to the compression stage (elements receiving the contents of buffer memory 18), in order to properly perform the encoding or compression of the input video signal comprised of picture data of a picture (field or frame), which includes motion prediction and other processes (see col. 13, lines 18-47). Other buffers are shown in elements 7, 8 and 26. Therefore, it would have been obvious to one of ordinary skill in the art of video processing and compression to have combined the Thomason reference, which teaches compression prior to storage, with the teachings of Yonemitsu et al, which teaches buffering the input signal prior to the compression stage for the advantages of storing picture or frame data in a buffer memory in order to perform the necessary encoding or compression operations, such as detecting a motion vector for motion prediction, in addition to actually compressing the stream and providing for smooth transmission of the stream after compression. One of ordinary skill in the art would have been led to make such a modification since buffering an input signal prior to the compression stage is well known in the art of video compression as described above. The claimed encoder configured to generate a first intermediate signal by compressing said video signal is met by Thomason as shown by data compressor 3 (Fig. 1, col. 3, lines 45-46), which generates the claimed first intermediate signal. The claimed controller separate from said encoder and

configured to (i) receive said first intermediate signal and (ii) present a second intermediate signal is met by elements 4, 31-33, 14 and 21-25 as shown in Fig. 1, where the first intermediate signal is received at buffers 4 and the second intermediate signal is presented at the output of buffers 14 and is sent to data decompressor or decoder 13. The claimed frame storage system directly connected to said controller and configured to (i) store said first intermediate signal and (ii) generate said second intermediate signal is met by buffer memory 35 and main memory 36 (Fig. 1, col. 3, line 53 – col. 4, line 40), which receives the first intermediate signal from 31 and the second intermediate is generated at the output data section of 35. The claimed time-shifted video decoder separate from said controller and configured to generate a second output signal by decompressing said second intermediate signal is met by data decompressor 13 (Fig. 1), which generates the second output signal that is sent through the acceleration control 41 and PIP/postprocessor 42 to a TV (col. 4, lines 15-40). The claimed wherein said controller is further configured to generate a command configured to control presenting (i) the first output signal when in the first mode and (ii) a second output signal when in a second mode is met by the live selection(s) path as shown in Fig. 1 for the first output signal, as well as the microprocessor 24 and the user command input ports 25 as part of the overall controller as described above, in conjunction with the acceleration control 41 and PIP/postprocessor 42 (see Fig. 1 and col. 3, line 58 – col. 4, line 40).

As to claim 16, the Thomason et al reference discloses the claimed apparatus as described above in claim 21. Thomason does not explicitly disclose that the encoder and the time-shifted decoder are provided in a single codec. However, the Examiner takes Official Notice that it is notoriously well known in the art of video distribution systems and recording apparatuses to

combine one or more hardware components into a single unit or software processing system for the advantage of making multiple parts integral together which may save size or space within the apparatus as well as reduce manufacturing costs for producing the apparatus. Therefore, it is submitted that it would have been clearly obvious to one of ordinary skill in the art at the time of the invention to have provided the encoder and the time-shifted decoder in a single codec for the advantages given above.

As to claim 28, although the Thomason et al reference does not explicitly disclose a frame buffer before the video encoder, the Examiner notes that it is well known in the art to have a frame buffer immediately before an encoder or compressor as shown by buffer memory 18 in Fig. 23 of the Yonemitsu et al reference (USPN 5,510,840).

As to claim 23, note the Thomason et al reference which discloses an apparatus (Fig. 1) for time-shifting a real-time video stream. The claimed input signal is met by the signals in arrow and channel selector 1 (see Fig. 1 and col. 3, lines 39-43). Although, the Thomason reference does not explicitly disclose a first frame buffer configured to generate a first signal and a second signal by buffering an input signal, pause said first signal at a frame during a transition form a real-time mode to a time-shifted mode and buffer a third signal, it is well known in the art to use a frame buffer in order to provide a smooth transition when switching between output signals for a change of mode, such as pausing a video output signal at a frame during transitions between modes. Moreover, Yonemitsu et al (USPN 5,510,840), clearly teaches that a frame buffer memory 18, as shown in Fig. 23, may be used at the input in order to provide a smooth transition when switching between signals for a change of mode, as well as providing buffering to account for variations in the timing of the video stream before reaching the compression stage.

The buffering (buffer memory 18) occurs just prior to the compression stage (elements receiving the contents of buffer memory 18), in order to properly perform the encoding or compression of the input video signal comprised of picture data of a picture (field or frame), which includes motion prediction and other processes (see col. 13, lines 18-47). Other buffers are shown in elements 7, 8 and 26, as well as buffer memory 18 receiving another signal (claimed "third") from control of the encoder 21. Therefore, it would have been obvious to one of ordinary skill in the art of video processing and compression to have combined the Thomason reference, which teaches compression prior to storage, with the teachings of Yonemitsu et al, which teaches buffering the input signal prior to the compression stage for the advantages of storing picture or frame data in a buffer memory in order to perform the necessary encoding or compression operations, such as detecting a motion vector for motion prediction, in addition to actually compressing the stream and providing for smooth transmission of the stream after compression. One of ordinary skill in the art would have been led to make such a modification since buffering an input signal prior to the compression stage is well known in the art of video compression as described above. In addition to, Yonemitsu et al discloses multiple buffer memory sections which may receive more than one input and the differences in the references and the claim are merely minor variations in schematics and are only a matter of semantics as related to the use of frame buffers, but not different in the overall functional use of the apparatus, and are not patentable distinctions as related to the Thomason et al and Yonemitsu et al references. The claimed controller...to receive said third signal is met by elements 4, 31-33, 14 and 21-25 of Thomason as combined with Yonemitsu (see Fig. 1), where the "third" signal is received at buffers 4 and the claimed buffer connected to said controller to store said third signal is met by

buffer memory 35 and main memory 36 (Fig. 1, col. 3, line 53 – col. 4, line 40), which receives the "third" signal from 31. The claimed encoder is met by Thomason as shown by data compressor 3 (Fig. 1, col. 3, lines 45-46), which generates the claimed third signal by compressing the second signal. The claimed decoder is met by data decompressor or decoder 13, which generates a fourth signal by decompressing said third signal as retrieved from said buffer (col. 4, lines 15-40). The claimed switch...configured to present an output signal comprising (i) said first signal when in said real-time mode and (ii) said fourth signal when in said time-shifted mode is met by the live selection(s) path as shown in Fig. 1 for the first signal, as well as the microprocessor 24 and the user command input ports 25 as part of the overall controller as described above, in conjunction with the acceleration control 41 and PIP/postprocessor 42 for the time-shifted mode (see Fig. 1 and col. 3, line 58 – col. 4, line 40).

As to claim 29, Thomason et al discloses a second frame buffer 14 between the rest of controller elements 4, 21-25 and 31-33, and time-shifted decoder 13, which buffers the "third" signal retrieved from buffer 35. Thomason et al does not explicitly disclose buffering said fourth signal prior to said switch with the same buffer. However, the difference between the reference and the claim is merely a minor variation in schematics and is only a matter of semantics as related to the use of frame buffers, moreover, the Yonemitsu et al reference as described above in claim 23, discloses multiple frame buffers that may have one or more inputs and outputs as shown in Fig. 23. Therefore, it would have been obvious to one of ordinary skill in the art to have further modified the Thomason et al reference with the Yonemitsu et al reference for the advantage of using portions of frame buffer memories in multiple paths in order to save hardware space and manufacturing costs.

As to claim 15, the claimed first processing path for said real-time mode is met by the live selection(s) path to the PIP/postprocessor 42 switch to the TV (Fig. 1) and the claimed second processing path for said time-shifted mode is through the a/d 2, the data compressor 3, etc... as shown in Fig. 1 and described in claim 21 and in col. 3, line 39 – col. 4, line 40.

As to claim 18, the Thomason et al reference does not explicitly disclose that the apparatus comprises a set-top box. However, the examiner takes Official Notice that it is notoriously well known in the art of video distribution systems to use set-top boxes with recoding and playback features for the advantage of consolidating a recoding device into a cable or satellite set-top box apparatus, which reduces the number of parts or devices used to perform the same tasks. Therefore, it is submitted that it would have been clearly obvious to one of ordinary skill in the art at the time of the invention to have used a set-top box for the advantages given above.

As to claim 19, the claimed output signal is viewable by an analog television is met by the TV, which receives the output signal from PIP/postprocessor 42 as shown in Fig. 1.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael W. Hoye whose telephone number is (571) 272-7346. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached at (571) 272-7353.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is **(571) 272-2600**.

Michael W. Hoye
May 20, 2005

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600